REMARKS

Applicant appreciates the examination of the present application that is evidenced by the Official Action of January 6, 2004. In response to the Official Action, Applicant has amended independent Claims 1, 4, 13 and 20 and dependent Claim 14 to highlight further aspects of the present invention that are not disclosed or suggested by the cited prior art. The substantive rejections to the claims based on Drapkin et al. and Partovi et al. will now be addressed.

Claims 1 and 4 are Patentable over Drapkin et al.

Applicant acknowledges that the gate terminal of the pass transistor **234** in FIG. 3 of Drapkin et al. is electrically connected by a reference signal line **132** to a floating level clamping circuit **124**, which includes a pair of diodes **240** and **242**. However, this reference signal line **132** appears to have a relatively high degree of capacitive loading on it, which can reduce the effectiveness of the capacitive bootstrapping effect that is present at the pass transistor **234** when the node **126** is switched high-to-low or low-to-high in response to corresponding switching of the I/O pad **104**. This high degree of capacitive loading on the reference signal line **132** is provided by the capacitance associated with the gate terminal of PMOS transistor **206**, the gate terminal of NMOS transistor **212** and the capacitive loading provided by the diodes within the floating level clamping circuit **124**. As illustrated by FIG. 3 of Drapkin et al., the PMOS transistor **206** operates as an element within an overshoot protection device **118** and the NMOS transistor **212** operates as an element within an undershoot protection device **120**.

In stark contrast to Drapkin et al., the gate terminal of the first pass transistor T3 in FIG. 3B of the present application has a relatively low degree of capacitive loading on it, which supports a high degree of capacitive bootstrapping at the first pass transistor T3 when the input terminal IN is switching high-to-low or low-to-high. This low degree of capacitive loading is present because the total capacitive loading on the signal line that connects the gate terminal of the first pass transistor T3 to the voltage clamping circuit **310** in FIG. 3B is provided by only two

relatively small NMOS transistors T1 and T2. The high degree of bootstrapping caused by the low degree of capacitive loading is described throughout the present application and, in particular, at pages 6 and 10-11 of the application:

> "According to an additional preferred aspect of this embodiment, a width of the first pass transistor is relatively large relative to the widths of the first and second NMOS transistors operating as diodes to thereby provided a high degree of capacitive coupling between the input and output signal lines and the gate of the first pass transistor. This high degree of capacitive coupling causes the voltage on the gate of the first pass transistor to immediately rise above the minimum clamped level as the input signal commences a transition from a logic 0 level to a logic 1 level.
>
> * * *
>
> The gate of the first pass transistor T3 is electrically connected to a preferred voltage clamping circuit **310**. The voltage clamping circuit **310** preferably occupies very limited area on an integrated circuit substrate and, as illustrated, may consist of first and second NMOS transistors T1 and T2 configured as MOS diodes. ... The first and second NMOS transistors T1 and T2 ... are preferably considerably narrower than the first and second pass transistors T3 and T4. The first and second NMOS transistors T1 and T2 are kept small so that their capacitance is low relative to the gate-to-channel capacitance of the first pass transistor T3.
>
> * * *
>
> However, because the width of the first pass transistor T3 is relatively large, the gate-to-channel capacitance across the first pass transistor T3 may provide a high degree of capacitive coupling between the gate of the first pass transistor T3 and its collective input (IN), output (OUT) and channel. This high degree of capacitive coupling will cause the voltage on the gate of the first pass transistor T3 to be "self-bootstrapped" up in voltage as the input signal Vin and the output signal Vout rise during a pull-up interval. The greater the width of the first pass transistor T3 relative to the first and second NMOS transistors T1 and T2 (clamping transistors) enhances the self-bootstrapping."

(See, e.g., '906 application, page 6, lines 14-22; page 10, lines 1-20; and page 11,

lines 8-20).

Claims 1 and 4 have been amended to reflect the low degree of capacitive loading on the signal line that electrically connects the gate terminal of the first pass transistor T3 to the voltage clamping circuit **310**. In particular, Claims 1 and 4 highlight how the total capacitive loading a gate of the first pass transistor T3 is less than two times the gate-to-channel capacitance of the first pass transistor T3. In other words, the total loading capacitance provided by the first and second MOS transistors T1 and T2 within the voltage clamping circuit **310** is less than the gate-to-channel capacitance of the first pass transistor T3.

In contrast to the subject matter recited by Claims 1 and 4, the total capacitance loading the gate terminal of the pass transistor **234** in FIG. 3 of Drapkin et al. is about equal to a sum of: (i) the gate-to-channel capacitance of the pass transistor **234**, (ii) the capacitive loading provided by the diodes **240** and **242**, (iii) the gate-to-channel capacitance of PMOS transistor **206**, and (iv) the gate-to-channel capacitance of NMOS transistor **212**. This high degree of capacitive loading reduces any bootstrapping effect at the pass transistor **234** and distinguishes Drapkin et al. from the subject matter of Claims 1 and 4.

Accordingly, Applicant respectfully submits that independent Claims 1 and 4 are patentable over Drapkin et al.

Claims 13 and 20 are Patentable over Drapkin et al. and Partovi et al.

Page 14 of the present application explains how a speed advantage can be achieved by adding a second pass transistor in the path between the input and output signal lines (IN and OUT). As illustrated by FIG. 3B and the timing diagram of FIG. 4 of the present application, faster pull-down characteristics can be achieved if a second pass transistor T4 is added to the overvoltage protection circuit. As described in the application, the value of $Vdd1-V_{TH-T4}$ can be set so that the second pass transistor T4 turns on before the first pass transistor T3 when the input signal line VIN is being switching high-to-low. Claims 13 and 20 reflect this aspect of the overvoltage protection circuit. For example, Claim 13 recites that

the first and second pass transistors (e.g., T3 and T4) are of same conductivity type (e.g., both are N-type) and that the "threshold voltage of said second pass transistor and the first power supply voltage are at values that cause said second pass transistor to turn on before said first pass transistor when the input signal line is switched high-to-low relative to the first power supply voltage." Claim 20 includes a similar recitation.

Applicant submits that FIG. 2 of Partovi et al. does not disclose or suggest "first and second pass transistors of same conductivity type." Instead, FIG. 2 of Partovi et al. merely discloses a CMOS transmission gate **109** containing an NMOS pass transistor **110** and a PMOS pass transistor **111** that is turned on whenever a control signal (e.g., output enable signal) is set high to enable a driver. Moreover, neither Partovi et al. nor Drapkin et al. disclose how the threshold voltage of the second pass transistor and the first power supply voltage are set at values "that cause said second pass transistor to turn on before said first pass transistor when the input signal line is switched high-to-low relative to the first power supply voltage."

Accordingly, Applicant submits that Claims 13 and 20 are patentable over the cited prior art references.

CONCLUSION

Applicant has amended all of the independent claims to highlight additional aspects of the present invention that are not disclosed or suggested by the cited prior art references. The amendments to Claims 1 and 4 highlight how a high degree of capacitive bootstrapping can be achieved at the gate of the first pass transistor T3 by using a voltage clamping circuit **310** that provides a very small capacitive load. The amendments to Claims 13 and 20 highlight how a faster pull-down characteristic can be achieved by using a second pass transistor T4 that is configured to turn on before the first pass transistor T3 when the input signal line IN switches high-to-low. These aspects of the amended claims are not disclosed or suggested by the cited prior art references. Accordingly, all independent claims are patentable and the application is now in condition for allowance. The

Examiner is encouraged to contact the undersigned by telephone in the event any outstanding issues remain that may prevent issuance of the present application.

Respectfully submitted,

Grant J. Scott
Registration No. 36,925

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401
#351304

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on January 19, 2004.

Candi L. Riggs
Date of Signature: January 19, 2004